DB Tester Board

Specification (v5)

S. Wu
J. Raaf – last modified 6 April 2007

The daughterboard tester is designed to simulate some features of the QB module.

SDS Control Functions

Various parameters of SDS may be controlled on the DB tester by writing to registers on the tester. Use EthDBlib functions EthUDPWrite() and EthUDPRead() to access these registers. See Table 1 for details.

Address	r/w	bit(s)	Description
0xe000	r/w	0-1	When '01', tester will generate sequential data When '10', tester will generate pseudo-random data (by LFSR) Otherwise, data written to 0x8000
	r/w	2	When '1', SDS always gets Q response (SDS never ends by Q)
	r/w	3	When '0', SDS burst length controlled by register 0xe002 When '1', SDS burst length is random (for random, maximum burst length can be set by register 0xe008)
	r/w	4	When '0', G_trig interval controlled by register 0xe004 When '1', G_trig occurs at random interval (for random, maximum interval can be set by register 0xe00a)
	r/w	5	When '0', SDSREQ interval controlled by register 0xe006 When '1', SDSREQ occurs at random interval (for random, maximum interval can be set by register 0xe00c
	r/w	6	When '0', force SDS burst length to multiple of 3 words (rounds up)
	r/w	7	When '1', enable JTAG programming of old (revision 1) DB
	r	8-15	DB Tester firmware version (read only)
0xe002	r/w	0-15	Set SDS burst length (minimum 2. If less than 2, still reads as 2)
0xe004	r/w	0-15	Set G_trig interval (in units of 150 ns)
0xe006	r/w	0-15	Set SDSREQ interval (in units of 150 ns)
0xe008	r/w	0-15	Random SDS burst length mask. Set bits 15 through N to '1' to limit maximum burst length to N-bits long
0xe00a	r/w	0-15	Random G_trig interval mask. Set bits 15 through N to '1' to limit maximum interval to N-bits long
0xe00c	r/w	0-15	Random SDSREQ interval mask. Set bits 15 through N to '1' to limit maximum interval to N-bits long

Table 1: SDS control registers

General Comments

All registers on tester will be reset by DB 'QB reset' command (UDP write 0x0080 to DB address 0x0000).

This version of tester firmware (v5) is designed for the revision 2 DBs. To program revision 1 DB with JTAG, bit 7 of register 0xe000 must be set to '1'.