# DB Tester Board

## Specification (v8)

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The daughterboard tester is designed to simulate some features of the QB module.

## SDS Control Functions

Various parameters of SDS may be controlled on the DB tester by writing to registers on the tester. Use EthDBlib functions EthUDPWrite() and EthUDPRead() to access these registers. See Table 1 for details.

## QB "Dummy Data" Emulation

If bits 1-0 in register 0xe000 are set to '11', the tester board will emulate the QB by producing "dummy data." In this case, SDS will be started by SDSREQ from QB. SDSREQ must be enabled on DB by writing '1' to bit 7 of DB register 0x106. See QB-DB Firmware Specification for details of DB registers.

Basic startup procedure for this mode:

1. Write '0' to register 0xe000
2. Write to register 0xe002 to set desired number of hits per event.
3. Set desired parameters of SDS in registers 0xe010-0xe018.
4. Write 0x3 to register 0xe000 to enable QB "dummy data" mode.
5. Start the test by writing 0x80 to register 0x106

| Address | r/w | bit(s) | Description |
|---|---|---|---|
| 0xe000 | r/w | 0-1 | When '01', tester will generate sequential data<br>When '10', tester will generate pseudo-random data (by LFSR)<br>When '11', special test format data (QB "dummy data" emulation).<br>In this mode, bits 2 and 6 (below) have no function, *i.e.*, Q is controlled by length and SDS burst length is always a multiple of 3.<br>See Table 2 for more information about this "dummy data" mode.<br>Otherwise, data written to 0x8000 |
| | r/w | 2 | When '1', SDS always gets Q response (SDS never ends by Q) |
| | r/w | 3 | When '0', SDS burst length controlled by register 0xe002<br>When '1', SDS burst length is random<br>(for random, maximum burst length can be set by register 0xe008) |
| | r/w | 4 | When '0', G_trig interval controlled by register 0xe004<br>When '1', G_trig occurs at random interval<br>(for random, maximum interval can be set by register 0xe00a) |
| | r/w | 5 | When '0', SDSREQ interval controlled by register 0xe006<br>When '1', SDSREQ occurs at random interval<br>(for random, maximum interval can be set by register 0xe00c |
| | r/w | 6 | When '0', force SDS burst length to multiple of 3 words (rounds up) |
| | r/w | 7 | When '1', enable JTAG programming of old (revision 1) DB |
| | r | 8-15 | DB Tester firmware version (read only) |
| 0xe002 | r/w | 0-15 | Set SDS burst length (minimum 2. If less than 2, still reads as 2)<br>When tester in QB "dummy data" mode (0xe000 set to 0x3), this register sets number of hits per event |
| 0xe004 | r/w | 0-15 | Set G_trig interval (in units of 150 ns) |
| 0xe006 | r/w | 0-15 | Set SDSREQ interval (in units of 150 ns) |
| 0xe008 | r/w | 0-15 | Random SDS burst length mask.<br>Set bits 15 through N to '1' to limit maximum burst length to N-bits long |
| 0xe00a | r/w | 0-15 | Random G_trig interval mask.<br>Set bits 15 through N to '1' to limit maximum interval to N-bits long |
| 0xe00c | r/w | 0-15 | Random SDSREQ interval mask.<br>Set bits 15 through N to '1' to limit maximum interval to N-bits long |

*Table 1: SDS control registers*

| Address | r/w | bit(s) | Description |
|---|---|---|---|
| 0xe010 | r/w | 0-15 | Number of hits per event (default = 4). Must be greater than or equal to parameter 'a' in register 0xe012. |
| 0xe012 | r/w | 0-15 | Parameter 'a', insert spacer cell after $a^{th}$ hit data cell. (default = 1) |
| 0xe014 | r/w | 0-15 | Parameter 'b' (should not be 0), (default = 2) |
| 0xe016 | r/w | 0-15 | Set LFSR starting state. Do not set to all '1'. (default = 0) |
| 0xe018 | r/w | 0-6 | Sets output data rate (units of 1 Mbit/s), (default = 0x50) |
| 0xe01a | r/w | 0-7 | Set non-zero values to use as tester ID. This ID will replace the high byte of the second word in sequential data cells, allowing the user to distinguish data from different testers (if ID is set to unique number for each tester). |

*Table 2: Registers for QB "dummy data" emulation. These registers are only used when register 0xe000 bits 0-1 are set to '11'*

## General Comments

All registers on tester will be reset by DB 'QB reset' command (UDP write 0x0080 to DB address 0x0000).

This version of tester firmware (v7) is designed for the revision 2 DBs. To program revision 1 DB with JTAG, bit 7 of register 0xe000 must be set to '1'.