QB-DB Firmware Specification
Firmware version 0x3a
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This document describes the firmware operation of the Ethernet Daughterboard for the QB for Super-K (QB-DB). The DB is controlled using a 100BaseT Ethernet interface implemented using SiTCP[SiTCP]. The QB-DB communicates with the QB using a variation of TKO protocol[TKO]. See Illustration 1 for a view of the DB layout facing the QB.

Note: This document describes firmware versions 0x10 and higher. This version of the document is based on firmware revision 0x3a. Previous test versions are significantly different.

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Ethernet Addresses

MAC Address - Each QB-DB provides its own unique Ethernet MAC address by means of a Dallas Semiconductor Silicon Serial Number™ (SSN) device. MAC addresses have the following format:

`00-50-51-xx-yy-zz`

where the final 3 bytes come from the SSN (the low two bits of zz are '0' as required by IEEE standard) QB-DB MAC addresses are in the range assigned to Iwatsu Electric (upper 24 bits 00-50-51 hex) which should avoid conflicts with commercial NICs, switches, etc).

I/P Address - Each QB-DB uses an IP address set using a combination of a fixed value of `192.168` programmed in firmware for the upper 16 bits, with the lower 12 bits supplied by a DIP switch on the QB-DB. Bits 12..15 are fixed as '0'. Switch assignments are given in Table 1 and marked on the silkscreen of the PCB (see Illustration 1 below).

Switch #	Function	I/P Bit
1	Slot# bit 0	0
2	Slot# bit 1	1
3	Slot# bit 2	2
4	Slot# bit 3	3
5	Slot# bit 4	4
6	Crate# bit 0	5
7	Crate# bit 1	6
8	Crate# bit 2	7
9	Crate# bit 3	8
10	Hut# bit 0	9
11	Hut# bit 1	10
12	Hut# bit 2	11

Table 1: I/P Address Switch Assignments
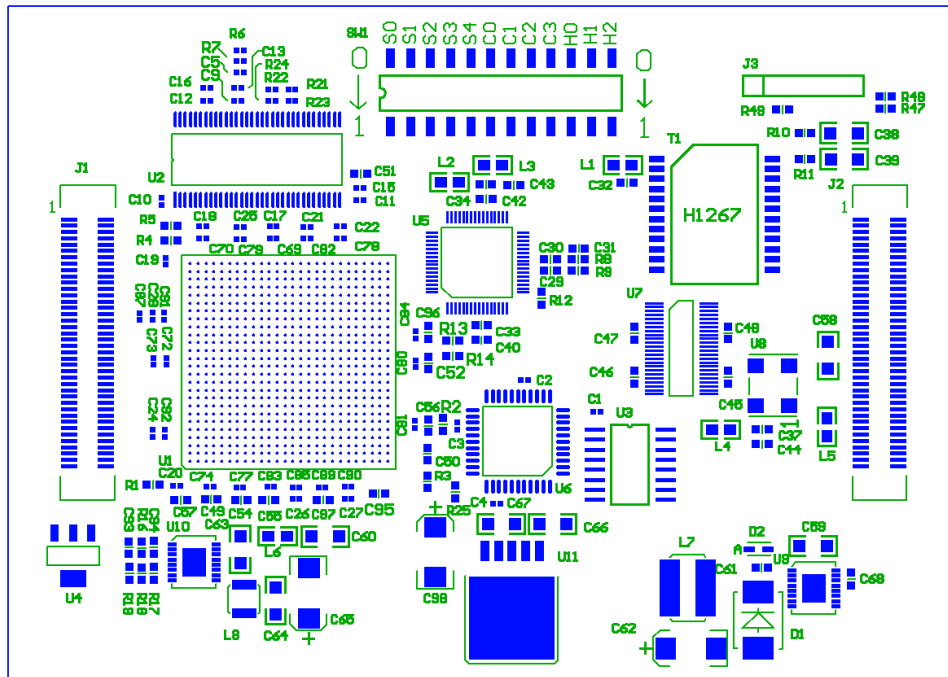
Illustration 1: QB-DB Layout (Side Facing QB)

UDP Protocol

Two protocols are supported by QB-DB. UDP datagrams may be sent to port `0x1234` to perform single register read/write operations. Each packet sent causes the QB-DB to send a return packet. Packets must conform to the BCP (board control protocol) defined in Table 2 below.

Byte Number	Name	Description
0	Ver.[3:0] / Type [3:0]	Should be 0xFF (test version)

1	Command[3:0] / Flag [3:0]	Command
		    0xC = Read operation
		    0x8 = Write operation
		Flag, valid only ACK packet
		    [3] = ACK packet
		    [2:1] = always zero
		    [0] = Bus error

2	ID	Number to identify packet, any number can be used.
3	Length	Length of read / write access

4	Address [31:24]	Read / Write Address
5	Address [23:16]	Read / Write Address
6	Address [15: 8]	Read / Write Address
7	Address [7: 0]	Read / Write Address
8	Write data [7:0]	1st write data
:		
7+N	Write data [7:0]	The last (N-th) write data

Table 2: Board Control Protocol

Address bits 31:16 are ignored. Addresses in the range 0x0000-0x7fff are reserved for on-board registers, while addresses in the range 0x8000-0xffff are used for TKO bus access (see Appendix A for details).

The data are always sent with most significant byte first (network byte order) in UDP operations. TCP operations are switchable to have either most significant byte first or least significant byte first.

TCP Protocol

A single TCP connection to port 0x17 may be opened to the QB-DB. Data are transmitted by the QB-DB under control of the SDS logic described below. Byte ordering of TCP data may be controlled by writing a bit in the DB status register 0x10a.

Sparse Data Scan (SDS)

SDS (sparse data scan) refers to the automatic transfer of data from QB FIFO via TKO read to the SiTCP transmit FIFO. It will be the primary means of data readout for the QB in normal operation.

A block diagram of the QB-DB emphasizing the data path is shown in Illustration 5 below. Data are transferred by SDS logic from the QB using TKO protocol and stored in the SDRAM buffer. Data are automatically copied from the SDRAM buffer to SiTCP transmit FIFO whenever a TCP connection is active and the SiTCP is not asserting the TX_FIFO_AFULL signal.

The SDRAM buffer provides a "buffer almost full" signal which is asserted when the buffer has a small amount of space remaining (~24 words), and de-asserted when the remaining space is large enough to contain a typical full QB worth of data (~1M words). For the remainder of this text this is referred to as the "buffer full" signal for simplicity.
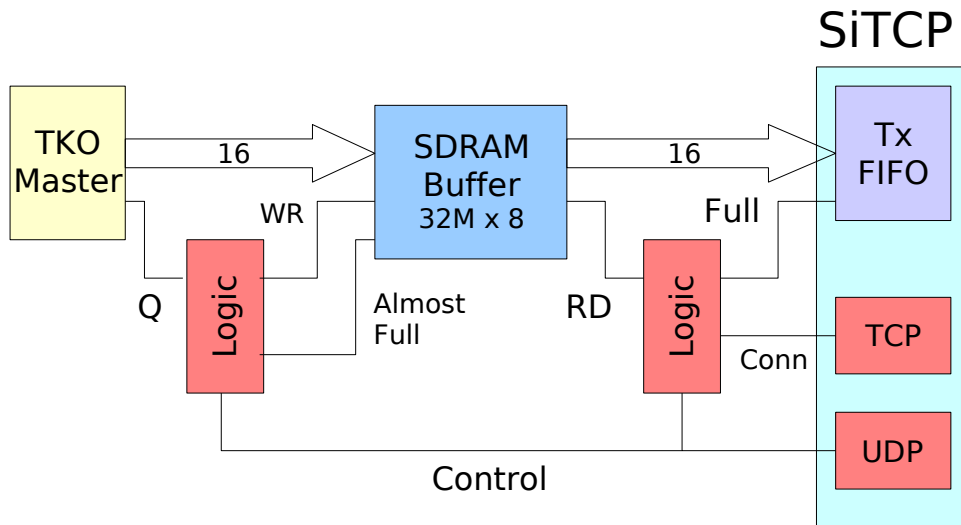
Illustration 2: QB-DB Block Diagram

SDS can be started by 4 methods:

- Periodic timer (programmable period ~ 1ms)

- Trigger counter (every n G_TRIG from QB)

- QB FIFO Threshold (dedicated SDSREQ signal from QB)

- UDP command (write bit in control register 0x104)

Once started, SDS logic will perform TKO read operations with (F=0, SA=0). As long as TKO Q=1, data are transferred to SDRAM buffer for TCP transmission via SiTCP. If an additional SDS start condition occurs while SDS is in progress, no action is taken. SDS will stop when one of the following occurs:

- TKO Q=0

- UDP command (write to bit 1 in control register 0x104 , for test only)

When SDS is enabled (any bit set in SDS enable register, address 0x106) or SDS transfer is in progress, TKO single action with F=0 or F=8 by UDP are prohibited. Any attempt to perform single action with F=0 or F=8 will fail and result in an error bit set (see page 11). Other TKO single action may be performed during SDS.

Note that when SDS is not enabled, TKO single action with F=0 may be used to read QB FIFO.

All data from QB are read out in 3-word cells. Each SDS transfer from QB will terminate (by Q=0) only after the end of a cell. If an SDS transfers a number of words which is not a multiple of 3, an error bit is set (see page 11).

One SDS may not exceed $2^{32}-1$ words. If this occurs, SDS is terminated and an error bit is set (see page

11).

Special cells are inserted in the data stream by the DB to flag start of SDS (header), end of SDS (trailer) or buffer full condition (warning).

Whenever an 'SDS start' condition occurs, all data are read from QB until Q=0 (or SDS is stopped by UDP operation). If there is space in the SDRAM buffer, data are stored in buffer, with header and trailer cells inserted before and after data. If there is no space in buffer, a warning cell is inserted in the buffer, and QB data is discarded. For a single SDS transfer one of the following actions may be taken:

1. Header, all data, trailer stored in buffer   [normal case]

2. Header cell and Warning cell stored in buffer,   [buffer full at start of SDS]
   all data discarded

3. Header, some data, trailer, warning cell stored,   [buffer full occurs during SDS]
   some data discarded

4. All data discarded, nothing stored in buffer   [buffer full at start of SDS,
                                               warning cell already stored]

After a warning cell is stored in the buffer, nothing else is stored until the buffer full signal turns off. The next cell stored will be the header for the start of the next SDS.

Illustration 3 below shows an example where there are four SDS start conditions. During the first, data is transferred to buffer as usual. During the second, the buffer full signal becomes active during the transfer. Data is discarded until the end of the SDS, where a trailer and warning cell are inserted. Then another SDS occurs where all data (including header and trailer) are discarded. Finally, the buffer full condition is cleared, and another SDS proceeds as usual.

TKO Bus	Data	Notes
	Header	SDS Start
Read Q=1	ATM Data	
Read Q=1	ATM Data	
Read Q=1	...	
Read Q=1	ATM Data	
Read Q=0	Trailer	SDS End
	Header	SDS Start
Read Q=1	ATM Data	
Read Q=1	ATM Data	Buffer full = 1
Read Q=1	...	Discard data
Read Q=0	Trailer	SDS End
	Warning	
Read Q=1		SDS Start
Read Q=1	...	Discard data
Read Q=0		SDS End
		Buffer full = 0
	Header	SDS Start
Read Q=1	ATM Data	
Read Q=1	ATM Data	
Read Q=1	...	
Read Q=1	ATM Data	
Read Q=0	Trailer	SDS End

Illustration 3: Sample Data Stream

QB Data Format Reference

All QB data consists of 3-word cells in the format shown below. The *header* field (bits 12-15) indicates the cell type.

Generic ATM Data Cell

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st Word	Header															
2nd Word																
3rd Word																

Header Value	Cell Type
0000-1011B	Hit data cell
1100B	Spacer cell
1110B	Status message cell
1111B	Cell inserted by DB

The QB cells (hit data, spacer and status message) are described in more detail in the QB documentation (add reference here). Cells with header = "1111" are generated by the daughterboard as described below.

Format of Header ("SDS Start") Cell

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st Word	Header				Type				Status				SeqNo[3:0]			
2nd Word	SeqNo[19:4]															
3rd Word	SeqNo[35:20]															

Header	1	1	1	1	Indicates cell inserted by DB

Type	0	0	0	1	Indicates summary information from DB

Status	0	0	0	1	Indicates SDS start

SeqNo		Incremented once for each SDS

A header cell is inserted in the buffer at the start of each SDS transfer (if the buffer is not full). The 36-bit SDS sequence number is incremented once for each SDS. If data are missing due to buffer overflow, the number of missing SDS can be determined by examining the sequence number.

Format of Trailer ("SDS Completed") Cell

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st Word	Header				Type				Status				Sequence #			
2nd Word	Word count for SDS (upper 16 bits)															
3rd Word	Word count for SDS (lower 16 bits)															

Header	1	1	1	1	Indicates cell inserted by DB

Type	0	0	0	1	Indicates summary information from DB

Status	0	0	1	0	Indicates SDS completed

Sequence #	-	-	-	-	Incremented once for each SDS

At the end of SDS, a trailer cell is inserted. The word count field contains a count of total words read in SDS. If buffer becomes full, some data may not be transferred to SiTCP, so the word count may not match the number of data words contained between header and trailer. Sequence number (4 bits only) should match low 4 bits of sequence number in header.

Format of Warning ("Nearly Full") Cell

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1st Word	Header				Type				Status				Sequence #			
2nd Word	Reserved															
3rd Word	Reserved															

Header	1	1	1	1	Indicates cell inserted by DB

Type	0	0	0	1	Indicates summary information from DB

Status	1	0	0	0	Indicates buffer nearly full

Sequence #	-	-	-	-	Not used?

A Warning cell is inserted when the buffer full signal becomes active (SDRAM buffer on daughterboard is almost full).

Appendix A - Control Registers on Daughterboard

Local registers on QB-DB are located in addresses from 0x0000-0x7fff. Note that all addresses not listed below are reserved, and any access to them may cause unexpected behavior.

All registers may be accessed using any length BCP operation, but most registers are 16 or 64 bits. All register data is transferred most significant byte first. All numbers are *hex* unless otherwise noted.

Address	r/w	bit(s)	Description
00	w	0	(mom) reset QB-DB (same as bits 1, 2, 3)
	w	1	(mom) reset TKO interface, SDRAM FIFO and counters 240-247
	w	2	(mom) reset error status bits (bits 12-15 of register 0x104)
	w	3	(mom) reset counters in range 120-125 and 200-27f except 240-247
		4-6	reserved
	w	7	(mom) reset QB board
	w	8	enable memory test mode (test only)
	w	9	enable SDS debug mode (test only)
	w	10	enable access to SPI interface on QB
		11-15	reserved
02	w	n/a	start flash operation (data ignored)
04	w	0-15	FPGA reload from flash write 00a5 to configure FPGA from default sector write 01a5 to configure FPGA from backup sector

Table 3: Command Registers (Addresses 00-04)

Note: Bits marked (mom) are momentary. When written as '1', they perform the specified action. These bits always read as '0'.

Address	r/w	bit(s)	Description
100	r/w	0-15	SDS start timer period (units of 100us). <mark>Period starts at end of last SDS.</mark>
102	r/w	0-15	SDS start after N+1 GTRG from QB. <mark>Count starts at end of last SDS.</mark>
104	r	0	SDS stopped by Q=0
	r	1	SDS stopped by UDP command
	r	2	SDS started by UDP command
	r	3	SDS started by G_trig
	r	4	SDS started by timer
	r	5	SDS started by SDSREQ
	r	6-7	reserved, read as '0'
	r	8	last TKO operation Q response
	r	9	last TKO operation YSSIR response
	r	10	SDRAM FIFO (almost) full
	r	11	SDS in progress
	r	12	SDS burst length counter has overflowed
	r	13	Q=0 occurred in middle of cell
	r	14	UDP read/write QB FIFO attempted while SDS enabled
	r	15	missing YSSIR response registered during SDS cycle
104	w	0	reserved, write as '0'
	w	1	stop SDS (test only)
	w	2	start SDS
	w	3-15	not used
106		0-3	reserved, write as '0'
	r/w	4	enable start SDS on G_trig (set to '0' at power-up)
	r/w	5	enable start SDS on timer (set to '0' at power-up)
	r/w	6	enable start SDS on UDP command (set to '0' at power-up)
	r/w	7	enable start SDS on SDSREQ from QB (set to '0' at power-up)
		8-15	reserved, write as '0'

Table 4: SDS Control/Status Registers (addresses 100-106)

Address	r/w	bit(s)	Description
108	r/w	0-15	Test register for exercising UDP read/write (test only)
10c	r	0-7	SDRAM DCM phase shift (test only)
	r	8-11	reserved, read as '0'
	r	12	SDRAM FIFO output empty (test only)
	r	13	SDRAM DCM phase control ready (test only)
	r	14	SDRAM initialization done (test only)
	r	15	SDRAM FIFO ready (test only)

Table 5: Test Registers (Addresses 108, 10c)

Address	r/w	bit(s)	Description
10a	r	0	DB FPGA configured from backup sector
	r	1	DB is in SDS debug mode (see Note 1)
	r	2	DB is in memory test mode (see Note 2)
	r	3	DB is in SPI access mode. Access QB flash via SPI instead of DB flash
	r	4	SDRAM FIFO (almost) full
	r	5	UDP acknowledge timeout occurred
	r	6-7	reserved, read as '0'
	r	8-10	inverted lock signal of DCM status on FPGA. Should be '0'
	r	11-12	reserved, read as '0'

	r/w	13	control TCP byte order
			   if '0' big-endian (most significant byte first)
			   if '1' little-endian (least significant byte first)

	r	14	TX_FIFO_AFULL signal from SiTCP
	r	15	TCP_ESTABLISH signal from SiTCP
140	r/w	0	MII_MAC_FLOW_ENABLE
	r/w	1	KEEP_ON
	r/w	2	FAST_RETRANS_ON
	r	3-15	All zero
142	r/w	0-15	KEEP_INTVL_FILL
144	r/w	0-15	KEEP_INTVL_EMPTY
146	r/w	0-15	TOUT_ESTB
148	r/w	0-15	TOUT_DISCNCT
14a	r/w	0-15	MSL
14c	r/w	0-15	Ethernet PHY data register
14e	r/w	0-4	Ethernet PHY command register number to be accessed

	r/w	5	'1' for write operation:
			   First write data to register 0x14c, then write '1' to bit 5 of 0x14e to
			   start write operation. Registers allowed for write: 0, 4, 7, 16
			'0' for read operation: Registers allowed for read: 0-8, 16-20, 30

	r/w	6	'1' if last operation succeeded
	r/w	7	'1' if last operation failed
	r	8-15	Not used
150	r/w	0-15	TOUT_RETRANS in units of microseconds
152	r/w	0-15	TX_BUF_TH

Table 6: DB Status Registers (Address 10a, 140-153)

Address	r/w	bit(s)	Description
10e	r	0-15	DB firmware version (0013 as of 2007-01-25)
110	r	0-15	SiTCP firmware version (bits 0-7 are month, bits 8-15 are year)
112	r	0-15	SiTCP firmware version (bits 0-7 are revision, bits 8-15 are day)
114	r	0-15	reserved, read as '0'
116	r	0	SSN readout done
	r	1	SSN CRC correct
	r	2-7	reserved, read as '0'
	r	8-15	calculated SSN CRC
118-11f	r	0-63	64 bit SSN readout value. Used to set MAC address (Note 3)

Table 7: Firmware Revisions and Serial Number (Addresses 10e-11f)

All counters described in Table 8 below are 64 bits. They may be read with any length UDP operation with the data always sent in MSB...LSB order. Counters will wrap at 0xffff ffff ffff ffff but this is unlikely!

Address	r/w	bit(s)	Description
120-121	r	0-3	Current SDS sequential number bits 32-35
		4-15	All zero
122-123	r	0-15	Current SDS sequential number bits 16-31
124-125	r	0-15	Current SDS sequential number bits 0-15
126-127	r	0-15	CRC-16 (=$x^{16} + x^{15} + x^2 + 1$) for data written to SiTCP
128-129	r	0-15	CRC-16(=$x^{16} + x^{15} + x^2 + 1$) for data written to SDRAM FIFO
200-207	r	0-63	Number of words written to SDRAM FIFO
208-20f	r	0-63	Total number of words SDS read from QB
210-217	r	0-63	Total number of SDS bursts
218-21f	r	0-63	Total number of words lost due to buffer full
220-227	r	0-63	number of SDS bursts completely lost due to buffer full
228-22f	r	0-63	number of SDS bursts partially lost due to buffer full
230-237	r	0-63	Total number of UDP bytes read or written (excluding address 230-23f)
238-23f	r	0-63	Total number of UDP bytes acknowledged (excluding address 230-23f)
240-247	r	0-63	number of words in SDRAM FIFO
248-24f	r	0-63	time SDRAM is empty from first write to SiTCP last write (40 ns units)
250-257	r	0-63	time TX_FIFO_AFULL is high from first write to last SiTCP to last write (40 ns units)
258-25f	r	0-63	total time elapsed from first write to SiTCP to last write (40 ns units)
260-267	r	0-63	total TCP connection time (40 ns units)
268-26f	r	0-63	total time with TCP_ESTABLISH=1 and TX_FIFO_AFULL=0
270-277	r	0-63	total number of bytes written to SiTCP
278-27f	r	0-63	total number of errors detected on pseudo-random data written to SiTCP

Table 8: Counter Registers (Addresses 120-125, 200-27f)

Notes:

1. In SDS debug mode, no flag cells are inserted. SDS halts when SDRAM FIFO is full.

2. In memory test mode, pseudo-random data written to SDRAM instead of SDS data. This data is generated by 16-bit (left-shift) LFSR, with bit 0 set to NOT(XOR(bits 15, 14, 12, 3)).

3. MAC address is 00 50 51 + SSN(bits 29-8) + 00.
   00 50 51 is prefix assigned to Iwatsu corporation. Remaining bits will be unique for each daughter board.

Flash Memory

Addresses from 400-7ff are used for the flash memory command and data buffer.

TKO Access

Addresses from 0x8000-0xffff are used for single-action access to TKO. Address bits are used as follows:

Address[15]	'1' for TKO operations.
Address[14:12]	TKO function code bits 2-0 (bit 3 is implied by read/write)
Address[11:1]	TKO sub-address bits 10-0
Address[0]	Always '0'

TKO function code bit '3' is set based on the type of operation requested using the BCP protocol.
For a write operation, bit '3' = 1
For a read operation, bit '3' = 0

Bibliography

SiTCP: T. Uchida, M. Tanaka, Development of a TCP/IP Processing Hardware, 2006, IEEE Nuclear Science Symposium,
TKO: KEK Data Acquisition Development Working Group, TKO Specification, 1985