Using Spartan 3E Starter Kit Board

upper 6 bits of serial signal
header = '1'
TDC on/off = '1' + sw3
Trigger mode = sw2 + sw1 + sw0
(control by switches)

6

serial signal =
upper 6 bits
+
low 32 bits (counter)

FPGA pins: D7
C7
F8
E8

32-bit counter
(increment every 38 clocks)

32

serial out
1 bit = 1 clock
start on falling edge

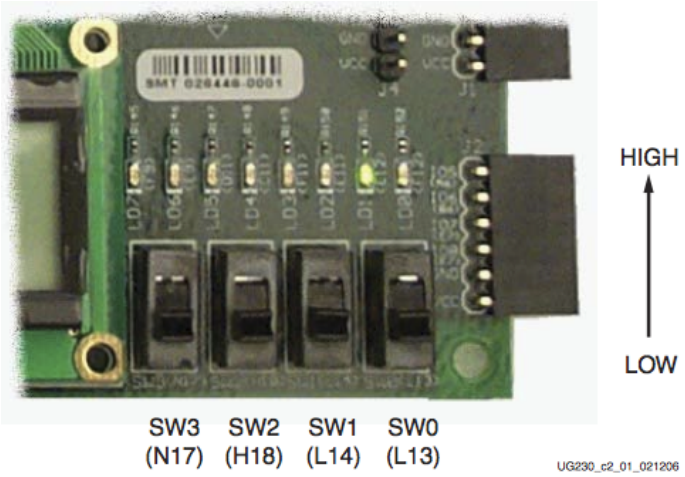
6-pin connector (J4)
and
Hirose 100-pin
connector (J3)

60 MHz
clock

50 MHz
on-board
crystal oscillator

DCM

FPGA pin: C9
Global buffer: GCLK10
Assoc. DCM: DCM_X0Y1



First 6 bits of serial signal:

switch 3 2 1 0

1	1	?	?	?	?

'1' if switched HIGH
'0' if switched LOW

(see MCLK output specification for details of serial signal bits)

Monitor pins for oscilloscope

6-pin male connector (J4)

D7 $\overline{\text{serial signal}}$
C7 serial signal
F8 $\overline{\text{60 MHz clock}}$
E8 60 MHz clock

6-pin female connector (J1)

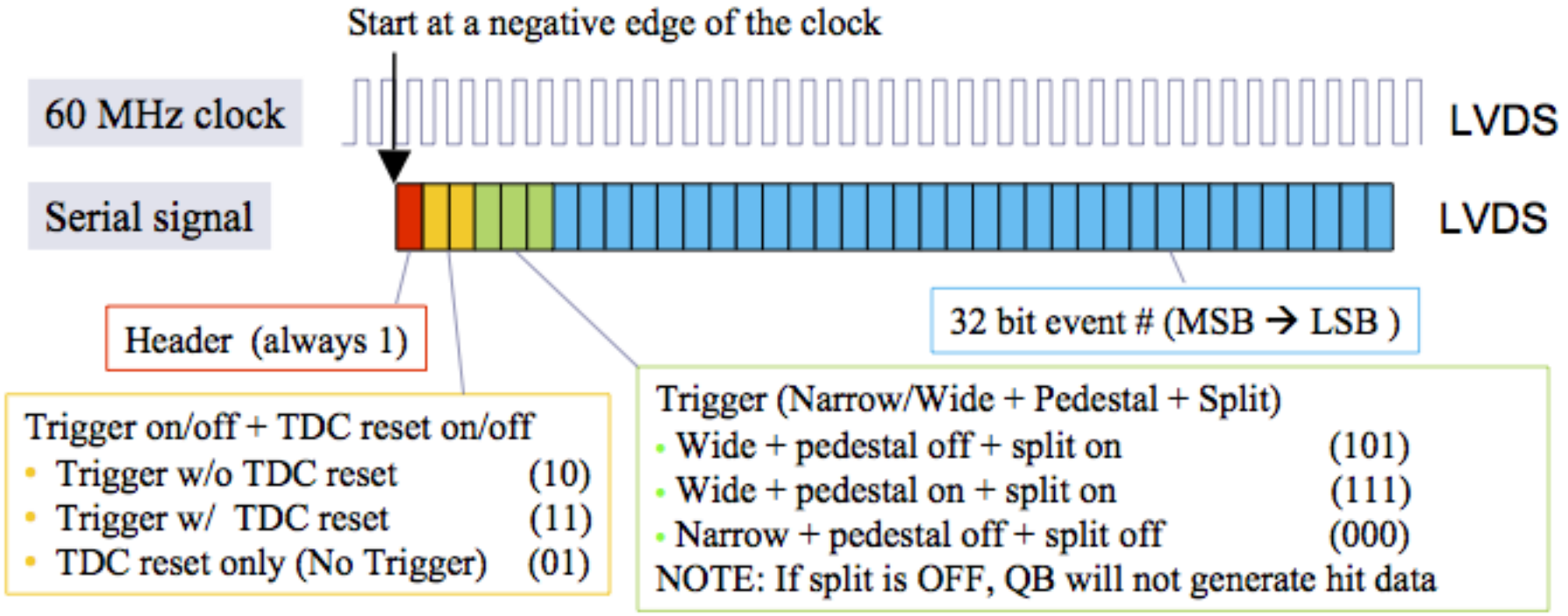
B4 50 MHz clock
A4
D5 reference bit (for triggering oscilloscope)
C5

6-pin female connector (J2)

A6
B6
E7
F7
GND ⌐ jumper in = no event number counter
VCC

MCLK output specification

- Output [2 pairs in 1 UTP cable]
  - (1,2) pair — 60 MHz clock
  - (5,6) pair — Trigger + 32 bit event # + TDC reset
  - (3,4) and (7,8)pairs — (not used, for future unification of CLK/TRG and 100BASE-TX)
- Spec. of serial signal [1 bit = 1 clock, total 38 clocks = 633 nsec]



"Read all the hits" mode sends serial signal once every 1024 clock cycles (every ~17 μs)